AMENDMENTS TO THE CLAIMS

1-30. (Cancelled)

31. (Previously Presented) A system comprising:

a bus;

a first host system coupled to the bus to control a first plurality of peripherals via the bus; and

a second host system coupled to the bus to control a second plurality of peripherals via the bus, wherein the first host system and the second host system each include a controller, the controller having a fault detection module coupled with fault detection hardware, the fault detection module to receive a notification from the fault detection hardware indicating a fault of either the first host system or the second host system, wherein when the fault occurs, the host system that failed suspends control of and disconnects from the bus, and the host system that is still active takes control of the plurality of peripheral devices coupled to the host that failed.

32. (Previously Presented) The system of claim 31, wherein the controller further comprises:

an interface to provide the controller with access to the first and second plurality of applications being executed on the first host system and the second host system;

a Peripheral Component Interconnect (PCI)-to-PCI (P2P) control module;

a power and reset control module; and

a clock control module to provide clock signals to the bus.

33. (Previously Presented) The system of claim 31, wherein the bus comprises a COMPACTPCI bus.

34. (Previously Presented) The system of claim 31 to use a Redundant System Slot (RSS) architecture.

35. (Previously Presented) The system of claim 32, wherein the first host system and the second host system each include a plurality communication modules, and an Ethernet link coupled with the plurality of communication modules to maintain synchronization between the first host system and the second host system.

36. (Previously Presented) The system of claim 31, wherein the first host system and the second host system each include a host control (HC) interface unit that is to:

receive control signals transmitted during startup and fail-over; and

respond to control signals transmitted during startup and fail-over.

37. (Previously Presented) A method comprising:

controlling a first plurality of peripherals on a first host system via a bus;

controlling a second plurality of peripherals on a second host system via the bus; and

receiving a notification from fault hardware indicating a fault of either the first host system or the second host system, wherein when the fault occurs, the host system that failed suspends control of and disconnects from the bus, and the host system that is still active takes control of the plurality of peripheral devices coupled to the host that failed.

38. (Previously Presented) The method of claim 37, further comprising:

accessing the first and second plurality of peripherals being executed on the first host system and the second host system; and

providing clock signals to the bus.

39. (Previously Presented) The method of claim 37, wherein the bus comprises a COMPACTPCI bus.

40. (Previously Presented) The method of claim 38, further comprising maintaining synchronization between the first host system and the second host system via an Ethernet link.

41. (Previously Presented) The method of claim 37, further comprising:

receiving control signals to be used during startup and fail-over; and

responding to the control signals received during startup and fail-over.

42-49. (Cancelled)